CYUSB302x

SD3™ USB and Mass Storage Peripheral Controller

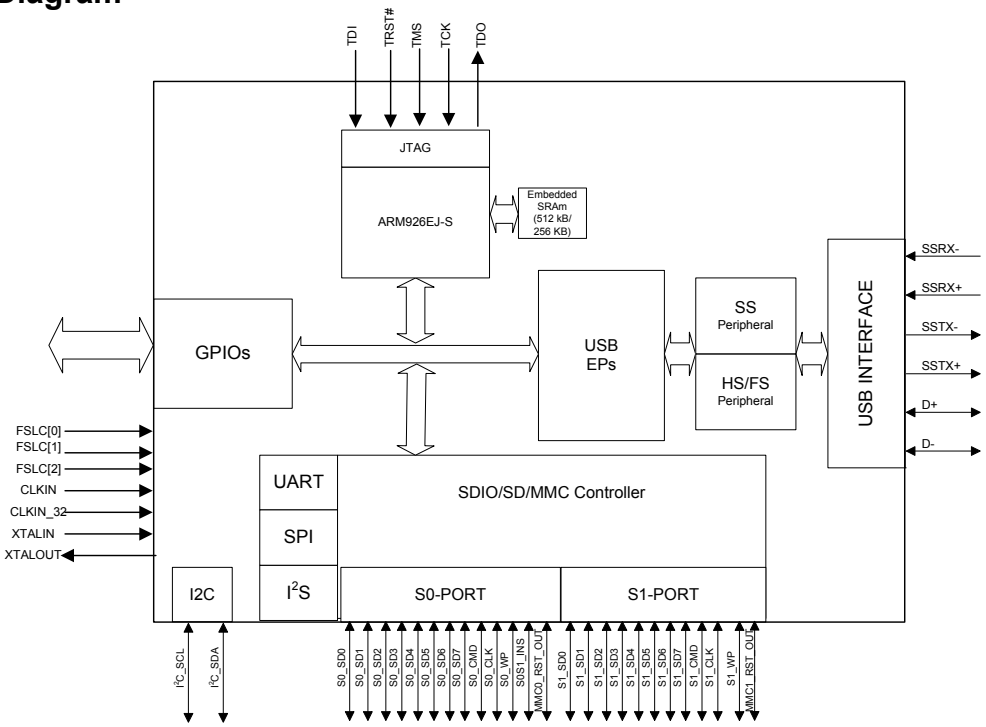
Features

- Latest-generation storage support
  - SD3.0/SDXC – UHS1 SDR50 / DDR50 Master
  - eMMC 4.4 Master
  - SDIO 3.0 Master
- USB integration
  - Certified USB 3.0 and USB 2.0 peripheral: SuperSpeed (SS), Hi-Speed (HS), and Full-Speed (FS) only)
  - Thirty-two physical endpoints
  - Integrated transceiver
  - Accessory charger adaptor (ACA) support
- Ultra low-power in core power-down mode
  - Less than 60 µA with VBATT on and 20 µA with VBATT off
- I^2C master controller at 1 MHz
- Selectable input clock frequencies
  - 19.2, 26, 38.4, and 52 MHz
  - 19.2-MHz crystal input support
- Independent power domains for core and I/O
- 10 × 10 mm, 0.8-mm pitch ball grid array (BGA) package
- 5.099 mm × 4.695 mm × 0.55 mm, with 0.4 mm pitch small footprint wafer-level chip scale package (WLCSP)

Applications

- USB thumb drives
- Card readers
- Laptop with SD slots
- SD slot in TV/STB
- WIFI Dongles
- USB SDIO Bridge
- Raid on-Chip Controller

Logic Block Diagram



Errata: For information on silicon errata, see "Errata" on page 30. Details include trigger conditions, devices affected, and proposed workaround.

Contents

Functional Overview

SD3™ is a USB 3.0 SuperSpeed mass-storage controller providing the latest SD/MMC support. SD3 complies with the SD Specification, Version 3.0, and the MMC Specification, Version 4.41.

SD3 offers the following access paths among USB and mass storage ports:

- A USB-port (U-Port) supporting USB 3.0 peripheral
- Two mass-storage ports (S0-Port and S1-Port) supporting mass-storage devices. Following are the possible configurations for the two mass-storage ports:
  - SD and MMC
  - SD and SD
  - MMC and MMC
  - SD and SDIO
  - MMC and SDIO
  - SDIO and SDIO

Combinations of these accesses can happen independently or in an interleaved manner.

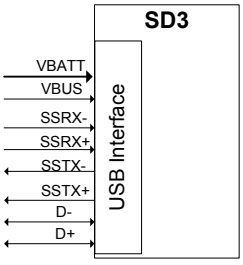
The SD3 complies with the USB 3.0 v1.0 specification and is also backward compatible with USB 2.0.

USB Interface (U-Port)

SD3 offers the following features:

- Supports USB peripheral functionality compliant with the USB 3.0 Specification Revision 1.0 and is backward-compatible with the USB 2.0 Specification
- Supports up to 16 IN and 16 OUT endpoints.
- Supports the USB 3.0 Streams feature. It also supports USB Attached SCSI (UAS) device class to optimize mass-storage access performance.
- As a USB peripheral, SD3 supports UAS and Mass Storage Class (MSC) peripheral classes.
- When the USB port is not in use, the PHY and transceiver may be disabled for power savings.

Figure 1. USB Interface Signals



Mass-Storage Support (S-Port)

The SD3 storage interface port supports the following specifications:

- SD Specification, Version 3.0
- Multimedia Card-System Specification, MMCA Technical Committee, Version 4.4
- SDIO Host controller compliant with SDIO Specification Version 3.00

I²C Interface

SD3 has an I²C interface compatible with the I²C Bus Specification Revision 3. Because SD3's I²C interface is capable of operating only as I²C master, it may be used to communicate with other I²C slave devices. For example, SD3 may boot from an EEPROM connected to the I²C interface, as a selectable boot option.

SD3's I²C master controller also supports multi-master mode functionality.

The power supply for the I²C interface is VIO5, which is a separate power domain from the other serial peripherals. This is to allow the I²C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I²C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I²C controller supports the clock stretching feature to enable slower devices to exercise flow control.

Both SCL and SDA signals of the I²C interface require external pull-up resistors. These resistors must be connected to VIO5.

UART Interface

The UART interface of SD3 supports full-duplex communication. It includes the signals noted in Table 1.

Table 1. UART Interface Signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then SD3's UART only transmits data when the CTS input is asserted. In addition to this, SD3's UART asserts the RTS output signal, when it is ready to receive data.

I²S Interface

SD3 has an I²S port to support external audio codec devices. SD3 functions as I²S Master as transmitter only. The I²S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). SD3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I²S interface are 32 kHz, 44.1 kHz, and 48 kHz.

SPI Interface

SD3 supports an SPI Master interface on the Serial Peripherals port. The maximum operation frequency is 33 MHz.

The SPI controller supports four modes of SPI communication (see SPI Timing Specification on page 21 for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from 4 bits to 32 bits.

Boot Options

SD3 can load boot images from various sources, selected by the configuration of the PMODE pins. The boot options for the SD3 are as follows:

- Boot from USB
- Boot from I^2C
- Boot from eMMC on S0-Port
- Boot from SPI

Table 2. Booting Options for SD3

PMODE[2:0] [1]	Boot From
FF0	S0-Port: eMMC On failure, USB boot enabled
FF1	USB Boot
FFF	I^2C On Failure, USB Boot is enabled
0FF	I^2C only
0F1	SPI On Failure, USB Boot is enabled

Reset

A reset is initiated by asserting the Reset# pin on SD3. The specific reset sequence and timing requirements are detailed in Figure 4 on page 18 and Table 14 on page 26. All I/Os are tristated during a hard reset.

Clocking

SD3 allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN_32 pins can be left unconnected if not used.

Crystal frequency supported is 19.2 MHz, while the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

SD3 has an on-chip oscillator circuit that uses an external 19.2 MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal option/clock frequency option. The configuration options are shown in Table 3.

Clock inputs to SD3 must meet the phase noise and jitter requirements specified in Table 4.

The input clock frequency is independent of the clock/data rate of SD3 core or any of the device interfaces. The internal PLL applies the appropriate clock multiply option depending on the input frequency.

Table 3. Crystal/Clock Frequency Selection

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/Clock Frequency
0	0	0	19.2-MHz crystal
1	0	0	19.2-MHz input CLK
1	0	1	26-MHz input CLK
1	1	0	38.4-MHz input CLK
1	1	1	52-MHz input CLK

Table 4. Input Clock Specifications for SD3

Parameter	Description	Specification		Units
		Min	Max	
Phase noise	100-Hz offset	–	–75	dB
	1-kHz offset	–	–104	dB
	10-kHz offset	–	–120	dB
	100-kHz offset	–	–128	dB
	1-MHz offset	–	–130	dB
Maximum frequency deviation	–	–	150	ppm
Duty cycle	–	30	70	%
Overshoot	–	–	3	%
Undershoot	–	–	–3	%
Rise time/fall time	–	–	3	ns

32-kHz Watchdog Timer Clock Input

SD3 includes a watchdog timer that can be used to interrupt the core, automatically wake up SD3 in Standby mode, and reset the core. The watchdog timer runs off a 32-kHz clock, which may optionally be supplied from an external source on a dedicated pin of SD3.

The watchdog timer can be disabled by firmware.

Requirements for the optional 32-kHZ clock input are listed in Table 5.

Table 5. 32-kHz Clock Input Requirements

Parameter	Min	Max	Units
Duty cycle	40	60	%
Frequency deviation	–	±200	ppm
Rise Time/fall Time	–	200	ns

Note
1. F indicates Floating.

Power

SD3 has the following main groups of power supply domains:

- **IO_VDDQ:** This refers to a group of independent supply domains for digital I/Os. The voltage level on these supplies are 1.8 V to 3.3 V. SD3 provides six independent supply domains for digital I/Os listed as follows:
  - S0VDDQ: S0-Port (for SD/MMC) I/O Power Supply Domain
  - S1VDDQ: S1-Port (for SD/MMC) I/O Power Supply Domain
  - S2VDDQ: S2-Port (GPIO) Power Supply Domain
  - VIO4: S1-Port GPIO[53:57]/O Power Supply Domain (these pins support MMC's high nibble data line - D[7:4] on S1-Port)
  - VIO5: I2C Power Supply Domain (supports 1.2 V to 3.3 V)
  - CVDDQ: Clock Power Supply Domain
- **VDD:** This is the supply voltage for the logic core. The nominal supply voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
  - **AVDD**: This is the 1.2-V supply for the PLL, crystal oscillator and other core analog circuits
  - **U3TXVDDQ/U3RXVDDQ**: These are the 1.2-V supply voltages for the USB 3.0 interface.
- **VBATT/VBUS:** This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through SD3's internal voltage regulator. VBATT is internally regulated to 3.3 V.

Power Modes

SD3 supports the following power modes:

- Normal mode: This is the full-functional operating mode. In this mode the internal CPU clock and the internal PLLs are enabled.

Normal operating power consumption does not exceed the sum of ICC_CORE max and ICC_USB max (see Table 9 on page 15 for current consumption specifications).

The I/O power supplies (S0VDDQ, S1VDDQ, VIO4, and VIO5) may be turned off when the corresponding interface is not in use. S2VDDQ cannot be turned off at any time if the S2-Port is used in the application.

- SD3 supports four low-power modes (see Table 6 on page 5):
  - Suspend mode with USB 3.0 PHY enabled (L1 mode)
  - Suspend mode with USB 3.0 PHY disabled (L2 mode)
  - Standby mode (L3 mode)
  - Core power-down mode (L4 mode)

Table 6. Entry and Exit Methods for Low-Power Modes

Low Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend mode with USB 3.0 PHY Enabled (L1 mode)	■ The power consumption in this mode does not exceed ISB_1 ■ USB 3.0 PHY is enabled and is in U3 mode (one of the suspend modes defined by the USB 3.0 specification). This one block alone operates with its internal clock while all other clocks are shut down ■ All I/Os maintain their previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory and all internal RAM are maintained ■ All transactions must be completed before SD3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on the core can put SD3 into suspend mode. For example, on USB suspend condition, firmware may decide to put SD3 into suspend mode	■ D+ transitioning to low or high ■ D– transitioning to low or high ■ Resume condition on SSRX +/- ■ Detection of VBUS ■ Assertion of GPIO[17] ■ Assertion of RESET#

Table 6. Entry and Exit Methods for Low-Power Modes (continued)

Low Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend mode with USB 3.0 PHY disabled (L2 mode)	■ The power consumption in this mode does not exceed ISB_2 ■ USB 3.0 PHY is disabled and the USB interface is in suspend mode ■ The clocks are shut off. The PLLs are disabled ■ All I/Os maintain their previous state ■ USB interface maintains the previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory, and all internal RAM are maintained ■ All transactions must be completed before SD3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on the core can put SD3 into suspend mode. For example, on USB suspend condition, firmware may decide to put SD3 into suspend mode	■ D+ transitioning to low or high ■ D– transitioning to low or high ■ Resume condition on SSRX +/- ■ Detection of VBUS ■ Assertion of GPIO[17] ■ Assertion of RESET#
Standby Mode (L3 mode)	■ The power consumption in this mode does not exceed ISB3 ■ All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor should take care that needed data is read before putting SD3 into this Standby Mode ■ The program counter is reset after waking up from Standby ■ GPIO pins maintain their configuration ■ Crystal oscillator is turned off ■ Internal PLL is turned off ■ USB transceiver is turned off ■ Core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually	■ Firmware executing on the core or external processor configures the appropriate register	■ Detection of VBUS ■ Assertion of GPIO[17] ■ Assertion of RESET#
Core Power Down Mode (L4 mode)	■ The power consumption in this mode does not exceed ISB_4 ■ Core power is turned off ■ All buffer memory, configuration registers and the program RAM do not maintain state. It is necessary to reload the firmware on exiting from this mode ■ In this mode, all other power domains can be turned on/off individually	■ Turn off VDD	■ Reapply VDD ■ Assertion of RESET#

Configuration Fuse

Fuse options are available for specific usage models. Contact Cypress Applications/Marketing for details.

Digital I/Os

SD3 provides firmware controlled pull-up or pull-down resistors internally on all digital I/O pins. The pins can be pulled high through an internal 50-kΩ resistor or can be pulled low through an internal 10-kΩ resistor to prevent the pins from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (through internal 50 kΩ)
- Pull down (through internal 10 kΩ)
- Hold (I/O hold its value) when in low power modes

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured based on each interface.

EMI

SD3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. SD3 can tolerate reasonable EMI, conducted by aggressor, outlined by these specifications and continue to function as expected.

System Level ESD

SD3 has built-in ESD protection on the D+, D–, GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-KV human body model (HBM) based on JESD22-A114 Specification
- ±6-KV contact discharge and ±8-KV air gap discharge based on IEC61000-4-2 level 3A
- ±8-KV contact discharge and ±15-KV air gap discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated.

The SuperSpeed USB signals (SSRX+, SSRX-, SSTX+, SSTX-) and S0/S1_INS have up to ±2.2 KV HBM internal ESD protection.

Pinout for BGA

Figure 2. SD3 BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	NC
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	NC	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	S1VDDQ	GPIO[49]	GPIO[48]	FSLC[2]	NC	NC	VDD	VBATT	VBUS
F	S0VDDQ	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	NC	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	S2VDDQ
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	NC	S2VDDQ	GPIO[11]	VSS

Pin Description for BGA

Table 7. Pin List

Pin No.	Power Domain	I/O	Name	Description		
S2-PORT (GPIO)						
F10	VI01	I/O	GPIO[0]	GPIO		
F9	VI01	I/O	GPIO[1]	GPIO		
F7	VI01	I/O	GPIO[2]	GPIO		
G10	VI01	I/O	GPIO[3]	GPIO		
G9	VI01	I/O	GPIO[4]	GPIO		
F8	VI01	I/O	GPIO[5]	GPIO		
H10	VI01	I/O	GPIO[6]	GPIO		
H9	VI01	I/O	GPIO[7]	GPIO		
J10	VI01	I/O	GPIO[8]	GPIO		
J9	VI01	I/O	GPIO[9]	GPIO		
K11	VI01	I/O	GPIO[10]	GPIO		
L10	VI01	I/O	GPIO[11]	GPIO		
K10	VI01	I/O	GPIO[12]	GPIO		
K9	VI01	I/O	GPIO[13]	GPIO		
J8	VI01	I/O	GPIO[14]	GPIO		
G8	VI01	I/O	GPIO[15]	GPIO		
J6	VI01	I/O	GPIO[16]	GPIO		
K8	VI01	I/O	GPIO[17]	GPIO		
K7	VI01	I/O	GPIO[18]	GPIO		
J7	VI01	I/O	GPIO[19]	GPIO		
H7	VI01	I/O	GPIO[20]	GPIO		
G7	VI01	I/O	GPIO[21]	GPIO		
G6	VI01	I/O	GPIO[22]	GPIO		
K6	VI01	I/O	GPIO[23]	GPIO		
H8	VI01	I/O	GPIO[24]	GPIO		
G5	VI01	I/O	GPIO[25]	GPIO		
H6	VI01	I/O	GPIO[26]	GPIO		
K5	VI01	I/O	GPIO[27]	GPIO		
J5	VI01	I/O	GPIO[28]	GPIO		
H5	VI01	I/O	GPIO[29]	GPIO		
G4	VI01	I/O	GPIO[30]	PMODE[0]		
H4	VI01	I/O	GPIO[31]	PMODE[1]		
L4	VI01	I/O	GPIO[32]	PMODE[2]		
L8			NC	No Connect		
C5	CVDDQ	I	RESET#	Active Low. Hardware Reset.		
				8b MMC Configuration	**SD+GPIO Configuration**	**GPIO Configuration**
K2	VI02	I/O	GPIO[33]	S0_SD0	S0_SD0	GPIO
J4	VI02	I/O	GPIO[34]	S0_SD1	S0_SD1	GPIO
K1	VI02	I/O	GPIO[35]	S0_SD2	S0_SD2	GPIO
J2	VI02	I/O	GPIO[36]	S0_SD3	S0_SD3	GPIO
J3	VI02	I/O	GPIO[37]	S0_SD4	GPIO	GPIO
J1	VI02	I/O	GPIO[38]	S0_SD5	GPIO	GPIO
H2	VI02	I/O	GPIO[39]	S0_SD6	GPIO	GPIO
H3	VI02	I/O	GPIO[40]	S0_SD7	GPIO	GPIO
F4	VI02	I/O	GPIO[41]	S0_CMD	S0_CMD	GPIO
G2	VI02	I/O	GPIO[42]	S0_CLK	S0_CLK	GPIO

Table 7. Pin List (continued)

Pin No.	Power Domain	I/O	Name	Description							
G3	VI02	I/O	GPIO[43]	S0_WP			S0_WP			GPIO	
F3	VI02	I/O	GPIO[44]	S0S1_INS			S0S1_INS			GPIO	
F2	VI02	I/O	GPIO[45]	MMC0_RST_OUT			GPIO			GPIO	
				8b MMC	**SD+UART**	**SD+SPI**	**SD+GPIO**	**GPIO**	**GPIO+ UART+I2S**	**SD+I2S**	**UART+ SPI+I2S**
F5	VI03	I/O	GPIO[46]	S1_SD0	S1_SD0	S1_SD0	S1_SD0	GPIO	GPIO	S1_SD0	UART_RTS
E1	VI03	I/O	GPIO[47]	S1_SD1	S1_SD1	S1_SD1	S1_SD1	GPIO	GPIO	S1_SD1	UART_CTS
E5	VI03	I/O	GPIO[48]	S1_SD2	S1_SD2	S1_SD2	S1_SD2	GPIO	GPIO	S1_SD2	UART_TX
E4	VI03	I/O	GPIO[49]	S1_SD3	S1_SD3	S1_SD3	S1_SD3	GPIO	GPIO	S1_SD3	UART_RX
D1	VI03	I/O	GPIO[50]	S1_CMD	S1_CMD	S1_CMD	S1_CMD	GPIO	I2S_CLK	S1_CMD	I2S_CLK
D2	VI03	I/O	GPIO[51]	S1_CLK	S1_CLK	S1_CLK	S1_CLK	GPIO	I2S_SD	S1_CLK	I2S_SD
D3	VI03	I/O	GPIO[52]	S1_WP	S1_WP	S1_WP	S1_WP	GPIO	I2S_WS	S1_WP	I2S_WS
D4	VIO4	I/O	GPIO[53]	S1_SD4	UART_RTS	SPI_SCK	GPIO	GPIO	UART_RTS	GPIO	SPI_SCK
C1	VIO4	I/O	GPIO[54]	S1_SD5	UART_CTS	SPI_SSN	GPIO	GPIO	UART_CTS	I2S_CLK	SPI_SSN
C2	VIO4	I/O	GPIO[55]	S1_SD6	UART_TX	SPI_MISO	GPIO	GPIO	UART_TX	I2S_SD	SPI_MISO
D5	VIO4	I/O	GPIO[56]	S1_SD7	UART_RX	SPI_MOSI	GPIO	GPIO	UART_RX	I2S_WS	SPI_MOSI
C4	VIO4	I/O	GPIO[57]	MMC1_RST_OUT	GPIO	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK
C9			NC	No Connect							
A3	U3RXVDDQ	I	SSRXM	USB 3.0 SuperSpeed Receive Minus							
A4	U3RXVDDQ	I	SSRXP	USB 3.0 SuperSpeed Receive Plus							
A6	U3TXVDDQ	O	SSTXM	USB 3.0 SuperSpeed Transmit Minus							
A5	U3TXVDDQ	O	SSTXP	USB 3.0 SuperSpeed Transmit Plus							
A9	VBATT/ VBUS	I/O	D+	USB (HS/FS) Data Plus							
A10	VBATT/ VBUS	I/O	D-	USB (HS/FS) Data Minus							
A11			NC	No Connect							
B2	CVDDQ	I	FSLC[0]	FSLC[0]							
C6	AVDD	I/O	XTALIN	XTALIN							
C7	AVDD	I/O	XTALOUT	XTALOUT							
B4	CVDDQ	I	FSLC[1]	FSLC[1]							
E6	CVDDQ	I	FSLC[2]	FSLC[2]							
D7	CVDDQ	I	CLKIN	CLKIN							
D6	CVDDQ	I	CLKIN_32	CLKIN_32							
D9	VIO5	I/O	I^2C_GPIO[58]	SCL (Serial Clock) for I^2C Bus Interface							
D10	VIO5	I/O	I^2C_GPIO[59]	SDA (Serial Data) for I^2C Bus Interface							
E7			NC	No Connect							
C10			NC	No Connect							
B11			NC	No Connect							
E8			NC	No Connect							
F6			NC	No Connect							
D11	VIO5	O	O[60]	Output only							
E10		PWR	VBATT								
B10		PWR	VDD								
A1		PWR	U3VSSQ								

Table 7. Pin List (continued)

Pin No.	Power Domain	I/O	Name	Description
E11		PWR	VBUS	
D8		PWR	VSS	
H11		PWR	S2VDDQ	
E2		PWR	VSS	
L9		PWR	S2VDDQ	
G1		PWR	VSS	
F1		PWR	S0VDDQ	
G11		PWR	VSS	
E3		PWR	S1VDDQ	
L1		PWR	VSS	
B1		PWR	VIO4	
L6		PWR	VSS	
B6		PWR	CVDDQ	
B5		PWR	U3TXVDDQ	
A2		PWR	U3RXVDDQ	
C11		PWR	VIO5	
L11		PWR	VSS	
A7		PWR	AVDD	
B7		PWR	AVSS	
C3		PWR	VDD	
B8		PWR	VSS	
E9		PWR	VDD	
B9		PWR	VSS	
F11		PWR	VDD	
H1		PWR	VDD	
L7		PWR	VDD	
J11		PWR	VDD	
L5		PWR	VDD	
K4		PWR	VSS	
L3		PWR	VSS	
K3		PWR	VSS	
L2		PWR	VSS	
A8		PWR	VSS	
				Precision Resistors
C8	VBUS/VBATT	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 kΩ+/-1% resistor between this pin and GND)
B3	U3TXVDDQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 Ω+/-1% resistor between this pin and GND)

Pinout for WLCSP

Figure 3. SD3 WLCSP Ball Map (Bottom View)[2]

	12	11	10	9	8	7	6	5	4	3	2	1
A	VSS	VSS	SSRXM		SSTXM	FSLC[0]	**AVSS**	**AVDD**	DP	U2AFEVSSQ	DM	**VDD**
B	L_GPIO[55]	LVDDQ	SSRXP	R_USB3	SSTXP	FSLC[2]	XTALIN	XTALOUT	SWDP	R_USB2	SWDM	**VDD**
C	L_GPIO[56]	S1VDDQ	U3RXVDDQ	U3VSSQ	U3TXVDDQ	CVDDQ	CLKIN_32	CLKIN	**U2PLLVSSQ**	OTG_ID	TDO	TRST#
D	S1_GPIO[49]	S1_GPIO[50]	L_GPIO[53]	L_GPIO[54]	RESET#	VDD	I2C_GPIO[58]	TMS	I2CVDDQ	TCK	I2C_GPIO[59]	VSS
E	L_GPIO[57]	S1_GPIO[48]	S1_GPIO[51]	S1_GPIO[52]	I2C_O[60]	VSS	VSS	VSS	VSS	P_GPIO[3]	**VBATT**	**VBUS**
F	VSS	S1_GPIO[46]	S1_GPIO[47]	FSLC[1]	TDI	VDD	VDD	VDD	VDD	P_GPIO[4]	P_GPIO[1]	P_GPIO[0]
G	S0VDDQ	S0_GPIO[43]	S0_GPIO[44]	S0_GPIO[45]	VSS	VSS	VDD	VSS	P_GPIO[9]	P_GPIO[7]	P_GPIO[6]	P_GPIO[2]
H	VSS	S0_GPIO[40]	S0_GPIO[41]	S0_GPIO[42]	S0_GPIO[39]	VSS	P_GPIO[20]	P_GPIO[18]	P_GPIO[14]	P_GPIO[12]	P_GPIO[8]	PVDDQ
J	S0VDDQ	S0_GPIO[38]	S0_GPIO[37]	S0_GPIO[36]	P_GPIO[31]	P_GPIO[27]	P_GPIO[25]	P_GPIO[22]	P_GPIO[19]	P_GPIO[15]	P_GPIO[10]	P_GPIO[5]
K	S0_GPIO[35]	S0_GPIO[34]	S0_GPIO[33]	P_GPIO[32]	P_GPIO[28]	P_GPIO[26]	P_GPIO[16]	P_GPIO[21]	INT#	P_GPIO[24]	P_GPIO[11]	VSS
L	VDD	VSS	VDD	P_GPIO[30]	P_GPIO[29]	PVDDQ	P_GPIO[23]	VSS	PVDDQ	P_GPIO[17]	P_GPIO[13]	VSS

Note
2. No ball is populated at location A9.

Pin Description for WLCSP

Table 8. Pin List

Pin	Power Domain	I/O	Name	Description		
				P-Port		
				GPIO		
F1	VI01	I/O	GPIO[0]	GPIO		
F2	VI01	I/O	GPIO[1]	GPIO		
G1	VI01	I/O	GPIO[2]	GPIO		
E3	VI01	I/O	GPIO[3]	GPIO		
F3	VI01	I/O	GPIO[4]	GPIO		
J1	VI01	I/O	GPIO[5]	GPIO		
G2	VI01	I/O	GPIO[6]	GPIO		
G3	VI01	I/O	GPIO[7]	GPIO		
H2	VI01	I/O	GPIO[8]	GPIO		
G4	VI01	I/O	GPIO[9]	GPIO		
J2	VI01	I/O	GPIO[10]	GPIO		
K2	VI01	I/O	GPIO[11]	GPIO		
H3	VI01	I/O	GPIO[12]	GPIO		
L2	VI01	I/O	GPIO[13]	GPIO		
H4	VI01	I/O	GPIO[14]	GPIO		
J3	VI01	I/O	GPIO[15]	GPIO		
K6	VI01	I/O	GPIO[16]	GPIO		
L3	VI01	I/O	GPIO[17]	GPIO		
H5	VI01	I/O	GPIO[18]	GPIO		
J4	VI01	I/O	GPIO[19]	GPIO		
H6	VI01	I/O	GPIO[20]	GPIO		
K5	VI01	I/O	GPIO[21]	GPIO		
J5	VI01	I/O	GPIO[22]	GPIO		
L6	VI01	I/O	GPIO[23]	GPIO		
K3	VI01	I/O	GPIO[24]	GPIO		
J6	VI01	I/O	GPIO[25]	GPIO		
K7	VI01	I/O	GPIO[26]	GPIO		
J7	VI01	I/O	GPIO[27]	GPIO		
K8	VI01	I/O	GPIO[28]	GPIO		
L8	VI01	I/O	GPIO[29]	GPIO		
L9	VI01	I/O	GPIO[30]	PMODE[0]		
J8	VI01	I/O	GPIO[31]	PMODE[1]		
K9	VI01	I/O	GPIO[32]	PMODE[2]		
K4	VI01	O	INT#	INT#		
D8	CVDDQ	I	RESET#	RESET#		
				S0-Port		
				8b MMC	**SD+GPIO**	**GPIO**
K10	VI02	I/O	GPIO[33]	S0_SD0	S0_SD0	GPIO
K11	VI02	I/O	GPIO[34]	S0_SD1	S0_SD1	GPIO
K12	VI02	I/O	GPIO[35]	S0_SD2	S0_SD2	GPIO
J9	VI02	I/O	GPIO[36]	S0_SD3	S0_SD3	GPIO
J10	VI02	I/O	GPIO[37]	S0_SD4	GPIO	GPIO
J11	VI02	I/O	GPIO[38]	S0_SD5	GPIO	GPIO
H8	VI02	I/O	GPIO[39]	S0_SD6	GPIO	GPIO
H11	VI02	I/O	GPIO[40]	S0_SD7	GPIO	GPIO
H10	VI02	I/O	GPIO[41]	S0_CMD	S0_CMD	GPIO

Table 8. Pin List (continued)

Pin	Power Domain	I/O	Name	Description							
H9	VI02	I/O	GPIO[42]	S0_CLK		S0_CLK		GPIO			
G11	VI02	I/O	GPIO[43]	S0_WP		S0_WP		GPIO			
G10	VI02	I/O	GPIO[44]	S0S1_INS		S0S1_INS		GPIO			
G9	VI02	I/O	GPIO[45]	MMC0_RST_OUT		GPIO		GPIO			
				S1-Port							
				8b MMC	**SD+UART**	**SD+SPI**	**SD+GPIO**	**GPIO**	**GPIO+UART+I2S**	**SD+I2S**	**UART+SPI+I2S**
F11	VI03	I/O	GPIO[46]	S1_SD0	S1_SD0	S1_SD0	S1_SD0	GPIO	GPIO	S1_SD0	UART_RTS
F10	VI03	I/O	GPIO[47]	S1_SD1	S1_SD1	S1_SD1	S1_SD1	GPIO	GPIO	S1_SD1	UART_CTS
E11	VI03	I/O	GPIO[48]	S1_SD2	S1_SD2	S1_SD2	S1_SD2	GPIO	GPIO	S1_SD2	UART_TX
D12	VI03	I/O	GPIO[49]	S1_SD3	S1_SD3	S1_SD3	S1_SD3	GPIO	GPIO	S1_SD3	UART_RX
D11	VI03	I/O	GPIO[50]	S1_CMD	S1_CMD	S1_CMD	S1_CMD	GPIO	I2S_CLK	S1_CMD	I2S_CLK
E10	VI03	I/O	GPIO[51]	S1_CLK	S1_CLK	S1_CLK	S1_CLK	GPIO	I2S_SD	S1_CLK	I2S_SD
E9	VI03	I/O	GPIO[52]	S1_WP	S1_WP	S1_WP	S1_WP	GPIO	I2S_WS	S1_WP	I2S_WS
D10	VI04	I/O	GPIO[53]	S1_SD4	UART_RTS	SPI_SCK	GPIO	GPIO	UART_RTS	GPIO	SPI_SCK
D9	VI04	I/O	GPIO[54]	S1_SD5	UART_CTS	SPI_SSN	GPIO	GPIO	UART_CTS	I2S_CLK	SPI_SSN
B12	VI04	I/O	GPIO[55]	S1_SD6	UART_TX	SPI_MISO	GPIO	GPIO	UART_TX	I2S_SD	SPI_MISO
C12	VI04	I/O	GPIO[56]	S1_SD7	UART_RX	SPI_MOSI	GPIO	GPIO	UART_RX	I2S_WS	SPI_MOSI
E12	VI04	I/O	GPIO[57]	MMC1_RST_OUT	GPIO	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK
				U-Port							
C3	VBUS/VBATT	I	OTG_ID	USB OTG Identification							
A10	U3RXVDDQ	I	SSRXM	USB 3.0 SuperSpeed Receive Minus							
B10	U3RXVDDQ	I	SSRXP	USB 3.0 SuperSpeed Receive Plus							
A8	U3TXVDDQ	O	SSTXM	USB 3.0 SuperSpeed Transmit Minus							
B8	U3TXVDDQ	O	SSTXP	USB 3.0 SuperSpeed Transmit Plus							
A4	VBUS/VBATT	I/O	DP	USB (HS/FS) Data Plus							
A2	VBUS/VBATT	I/O	DM	USB (HS/FS) Data Minus							
B4	VBUS/VBATT	I/O	SWDP	USB (HS/FS) Switch Interface Data Plus							
B2	VBUS/VBATT	I/O	SWDM	USB (HS/FS) Switch Interface Data Minus							
				Crystal/Clocks							
A7	CVDDQ	I	FSLC[0]	Frequency Select 0							
B6	AVDD	I/O	XTALIN	Crystal Oscillator Input							
B5	AVDD	I/O	XTALOUT	Crystal Oscillator Output							
F9	CVDDQ	I	FSLC[1]	Frequency Select 1							
B7	CVDDQ	I	FSLC[2]	Frequency Select 2							
C5	CVDDQ	I	CLKIN	External Clock Input							
C6	CVDDQ	I	CLKIN_32	32.76-kHz Clock Input for Watchdog Timer							
				Other							
D6	I2C_VDDQ	I/O	I2C_GPIO[58]	SCL (Serial Clock) for I^2C Bus Interface							
D2	I2C_VDDQ	I/O	I2C_GPIO[59]	SDA (Serial Data) for I^2C Bus Interface							
F8	I2C_VDDQ	I	TDI	TDI (Test Data In) for JTAG Interface							
C2	I2C_VDDQ	O	TDO	TDO (Test Data Out) for JTAG Interface							
C1	I2C_VDDQ	O	TRST#	TRST (Test Reset) for JTAG Interface							
D5	I2C_VDDQ	O	TMS	TMS (Test Mode Select) for JTAG Interface							
D3	I2C_VDDQ	O	TCK	TCK (Test Clock) for JTAG Interface							
E8	I2C_VDDQ	O	O[60]	Charger Detect Output							
				Power							
E2		PWR	VBATT	USB Supply Voltage Input							

Table 8. Pin List (continued)

Pin	Power Domain	I/O	Name	Description
B1		PWR	VDD	
A1		PWR	VDD	
C9		PWR	U3VSSQ	GND
E1		PWR	VBUS	USB Supply Voltage Input
C4		PWR	U2PLLVSSQ	USB2 Regulator GND
H1		PWR	PVDDQ	P-Port Supply Voltage Input
K1		PWR	VSS	GND
L4		PWR	PVDDQ	P-Port Supply Voltage Input
L5		PWR	VSS	GND
L7		PWR	PVDDQ	P-Port Supply Voltage Input
L1		PWR	VSS	GND
J12		PWR	S0VDDQ	S0-Port Supply Voltage Input
H12		PWR	VSS	GND
G12		PWR	S0VDDQ	S0- Port Supply Voltage Input
C11		PWR	S1VDDQ	S1-Port Supply Voltage Input
F12		PWR	VSS	GND
B11		PWR	LVDDQ	Low Performance Peripherals Supply Voltage Input
A11		PWR	VSS	GND
A12		PWR	VSS	GND
C7		PWR	CVDDQ	Clock Supply Voltage Input
C8		PWR	U3TXVDDQ	USB3 1.2V Supply Voltage
C10		PWR	U3RXVDDQ	USB3 1.2V Supply Voltage
D4		PWR	I2C_VDDQ	I2C and JTAG Supply Voltage Input
A3		PWR	U2AFEVSSQ	GND
A5		PWR	AVDD	Analog Supply Voltage Input
A6		PWR	AVSS	Analog GND
F4		PWR	VDD	Core Supply Voltage Input
D1		PWR	VSS	GND
F5		PWR	VDD	Core Supply Voltage Input
E4		PWR	VSS	GND
F6		PWR	VDD	Core Supply Voltage Input
E5		PWR	VSS	GND
F7		PWR	VDD	Core Supply Voltage Input
E6		PWR	VSS	GND
D7		PWR	VDD	Core Supply Voltage Input
E7		PWR	VSS	GND
G6		PWR	VDD	Core Supply Voltage Input
L10		PWR	VDD	Core Supply Voltage Input
L12		PWR	VDD	Core Supply Voltage Input
H7		PWR	VSS	GND
G7		PWR	VSS	GND
L11		PWR	VSS	GND
G8		PWR	VSS	GND
G5		PWR	VSS	GND
B3	VBUS/VBATT	I/O	R_USB2	Precision Resistor for USB 2.0 (Connect a 6.04 kΩ ± 1% resistor between this pin and GND)
B9	U3TXVDDQ	I/O	R_USB3	Precision Resistor for USB 3.0 (Connect a 200Ω ± 1% resistor between this pin and GND)

AC Timing Parameters

Storage Port Timing

The S0-Port and S1-Port support the MMC Specification Version 4.4 and SD Specification Version 3.0.

Table 9 lists the timing parameters for S0-Port and S1-Port of SD3.

Table 9. S-Port Timing Parameters[3]

Parameter	Description	Min	Max	Units
MMC-20				
tSDIS CMD	Host input setup time for CMD	4.8	–	ns
tSDIS DAT	Host input setup time for DAT	4.8	–	ns
tSDIH CMD	Host input hold time for CMD	4.4	–	ns
tSDIH DAT	Host input hold time for DAT	4.4	–	ns
tSDOS CMD	Host output setup time for CMD	5	–	ns
tSDOS DAT	Host output setup time for DAT	5	–	ns
tSDOH CMD	Host output hold time for CMD	5	–	ns
tSDOH DAT	Host output hold time for DAT	5	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	50	–	ns
SDFREQ	Clock frequency		20	MHz
tSDCLKOD	Clock duty cycle	40	60	%
MMC-26				
tSDIS CMD	Host input setup time for CMD	10	–	ns
tSDIS DAT	Host input setup time for DAT	10	–	ns
tSDIH CMD	Host input hold time for CMD	9	–	ns
tSDIH DAT	Host input hold time for DAT	9	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	3	–	ns
tSDOH DAT	Host output hold time for DAT	3	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	38.5	–	ns
SDFREQ	Clock frequency		26	MHz
tSDCLKOD	Clock duty cycle	40	60	%
MC-HS				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	4	–	ns
tSDIH CMD	Host input hold time for CMD	3	–	ns
tSDIH DAT	Host input hold time for DAT	3	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	3	–	ns
tSDOH DAT	Host output hold time for DAT	3	–	ns
tSCLKR	Clock rise time	–	2	ns

Table 9. S-Port Timing Parameters[3] (continued)

Parameter	Description	Min	Max	Units
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	19.2	–	ns
SDFREQ	Clock frequency	–	52	MHz
tSDCLKOD	Clock duty cycle	40	60	%
MMC-DDR52				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	0.56	–	ns
tSDIH CMD	Host input hold time for CMD	3	–	ns
tSDIH DAT	Host input hold time for DAT	2.58	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	2.5	–	ns
tSDOH CMD	Host output hold time for CMD	3	–	ns
tSDOH DAT	Host output hold time for DAT	2.5	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	19.2	–	ns
SDFREQ	Clock frequency		52	MHz
tSDCLKOD	Clock duty cycle	45	55	%
SD-Default Speed (SDR12)				
tSDIS CMD	Host input setup time for CMD	24	–	ns
tSDIS DAT	Host input setup time for DAT	24	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	5	–	ns
tSDOS DAT	Host output setup time for DAT	5	–	ns
tSDOH CMD	Host output hold time for CMD	5	–	ns
tSDOH DAT	Host output hold time for DAT	5	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	40	–	ns
SDFREQ	Clock frequency		25	MHz
tSDCLKOD	Clock duty cycle	40	60	%
SD-High-Speed(SDR25)				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	4	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	6	–	ns
tSDOS DAT	Host output setup time for DAT	6	–	ns
tSDOH CMD	Host output hold time for CMD	2	–	ns
tSDOH DAT	Host output hold time for DAT	2	–	ns
tSCLKR	Clock rise time	–	2	ns

Table 9. S-Port Timing Parameters[3] (continued)

Parameter	Description	Min	Max	Units
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	20	–	ns
SDFREQ	Clock frequency	–	50	MHz
tSDCLKOD	Clock duty cycle	40	60	%
SD-SDR50				
tSDIS CMD	Host input setup time for CMD	1.5	–	ns
tSDIS DAT	Host input setup time for DAT	1.5	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	0.8	–	ns
tSDOH DAT	Host output hold time for DAT	0.8	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	10	–	ns
SDFREQ	Clock frequency		100	MHz
tSDCLKOD	Clock duty cycle	40	60	%
SD-DDR50				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	0.92	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	6	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	0.8	–	ns
tSDOH DAT	Host output hold time for DAT	0.8	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	20	–	ns
SDFREQ	Clock frequency		50	MHz
tSDCLKOD	Clock duty cycle	45	55	%

Note
3. All parameters guaranteed by design and validated through characterization.

I²C Interface Timing

I²C Timing

Figure 4. I²C Timing Definition

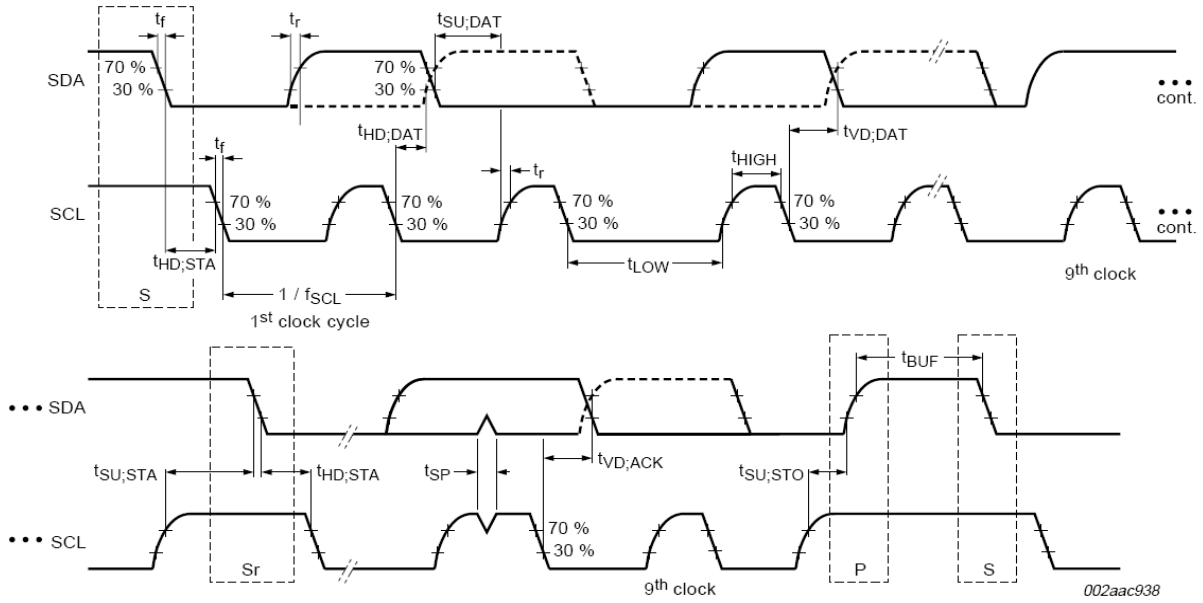


Table 10. I²C Timing Parameters[4]

Parameter	Description	Min	Max	Units
I²C Standard Mode Parameters				
fSCL	SCL clock frequency	0	100	kHz
tHD:STA	Hold time START condition	4	–	µs
tLOW	LOW period of the SCL	4.7	–	µs
tHIGH	HIGH period of the SCL	4	–	µs
tSU:STA	Setup time for a repeated START condition	4.7	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	250	–	ns
tr	Rise time of both SDA and SCL signals	–	1000	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	4	–	µs
tBUF	Bus free time between a STOP and START condition	4.7	–	µs
tVD:DAT	Data valid time	–	3.45	µs
tVD:ACK	Data valid ACK	–	3.45	µs
tSP	Pulse width of spikes that must be suppressed by input filter	n/a	n/a	

Note
4. All parameters guaranteed by design and validated through characterization.

Table 10. I²C Timing Parameters[4] (continued)

Parameter	Description	Min	Max	Units
I²C Fast Mode Parameters				
fSCL	SCL clock frequency	0	400	kHz
tHD:STA	Hold time START condition	0.6	–	µs
tLOW	LOW period of the SCL	1.3	–	µs
tHIGH	HIGH period of the SCL	0.6	–	µs
tSU:STA	Setup time for a repeated START condition	0.6	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	100	–	ns
tr	Rise time of both SDA and SCL signals	–	300	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	0.6	–	µs
tBUF	Bus-free time between a STOP and START condition	1.3	–	µs
tVD:DAT	Data valid time	–	0.9	µs
tVD:ACK	Data valid ACK	–	0.9	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns
I²C Fast Mode Plus Parameters (Not supported at I2C_VDDQ = 1.2V)				
fSCL	SCL clock frequency	0	1000	kHz
tHD:STA	Hold time START condition	0.26	–	µs
tLOW	LOW period of the SCL	0.5	–	µs
tHIGH	HIGH period of the SCL	0.26	–	µs
tSU:STA	Setup time for a repeated START condition	0.26	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	50	–	µs
tr	Rise time of both SDA and SCL signals	–	120	ns
tf	Fall time of both SDA and SCL signals	–	120	ns
tSU:STO	Setup time for STOP condition	0.26	–	µs
tBUF	Bus free time between a STOP and START condition	0.5	–	µs
tVD:DAT	Data valid time	–	0.45	µs
tVD:ACK	Data valid ACK	–	0.55	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

I²S Timing Diagram

Figure 5. I²S Transmit Cycle

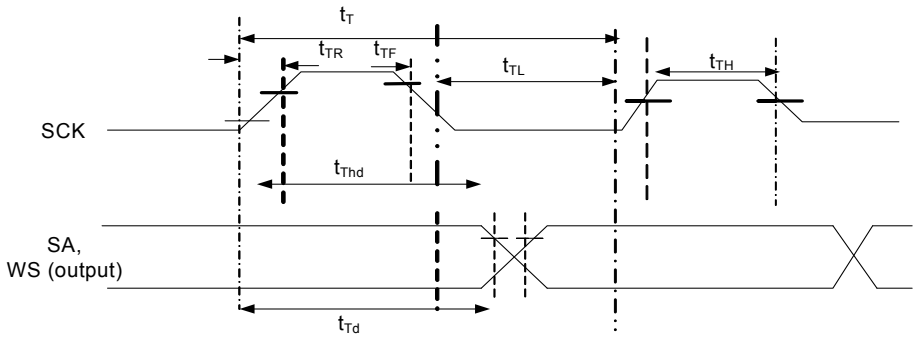


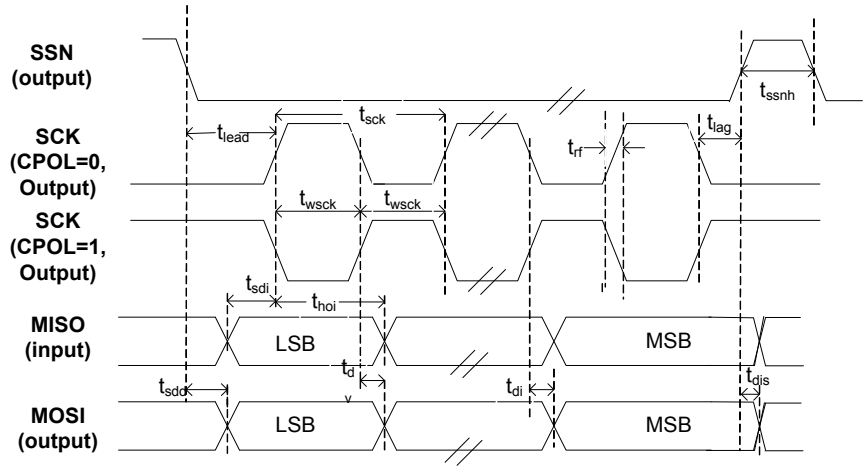
Table 11. I²S Timing Parameters[5]

Parameter	Description	Min	Max	Units
tT	I²S transmitter clock cycle	Ttr	–	ns
tTL	I²S transmitter cycle LOW period	0.35 Ttr	–	ns
tTH	I²S transmitter cycle HIGH period	0.35 Ttr	–	ns
tTR	I²S transmitter rise time	–	0.15 Ttr	ns
tTF	I²S transmitter fall time	–	0.15 Ttr	ns
tThd	I²S transmitter data hold time	0	–	ns
tTd	I²S transmitter delay time	–	0.8tT	ns
Note tT is selectable through clock gears. Max Ttr is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).				

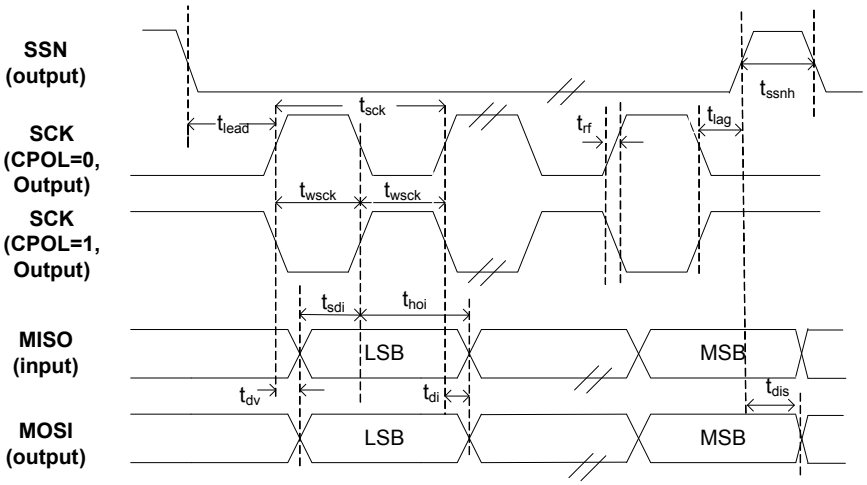
Note
5. All parameters guaranteed by design and validated through characterization.

SPI Timing Specification

Figure 6. SPI Timing



SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

Table 12. SPI Timing Parameters[6]

Parameter	Description	Min	Max	Units
fop	Operating frequency	0	33	MHz
tsck	Cycle time	30	–	ns
twsck	Clock high/low time	13.5	–	ns
tlead	SSN-SCK lead time	1/2 tsck[7]-5	1.5 tsck[7]+ 5	ns
tlag	Enable lag time	0.5	1.5 tsck[7]+5	ns
trf	Rise/fall time	–	8	ns
tsdd	Output SSN to valid data delay time	–	5	ns
tdv	Output data valid time	–	5	ns
tdi	Output data invalid	0	–	ns
tssnh	Minimum SSN high time	10	–	ns
tsdi	Data setup time input	8	–	ns
thoi	Data hold time input	0	–	ns
tdis	Disable data output on SSN high	0	–	ns

Notes
6. All parameters guaranteed by design and validated through characterization.
7. Depends on LAG and LEAD setting in the SPI_CONFIG register.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Supply voltage to ground potential V_{DD}, A_{VDDQ} ..... 1.25 V

$S2_{VDDQ}$,$S1_{VDDQ}$, $S0_{VDDQ}$, V_{IO4}, V_{IO5} ..... 3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ ..... 1.25 V

DC input voltage to any input pin ..... VCC + 0.3

DC voltage applied to outputs in High Z State ..... VCC + 0.3

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ±2.2-KV human body model (HBM) based on JESD22-A114
- Additional ESD Protection levels on D+, D–, VBUS, GND pins U-port and GPIO pins LPP-Port
- ±6-KV contact discharge, ±8-KV air gap discharge based on IEC61000-4-2 level 3A, ±8-KV contact discharge, and ±15-KV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current ..... > 200 mA

Maximum output short circuit current for all I/O configurations. (Vout = 0 V) ..... –100 mA

Operating Conditions

TA (ambient temperature under bias) Industrial ..... –40 °C to +85 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$ supply voltage ..... 1.15 V to 1.25 V

V_{BATT} supply voltage ..... 3.2 V to 6 V

$S2_{VDDQ}$, $S1_{VDDQ}$, $S0_{VDDQ}$, V_{IO4}, C_{VDDQ} supply voltage ..... 1.7 V to 3.6 V

V_{IO5} supply voltage ..... 1.15 V to 3.6 V

DC Specifications

Table 13. DC Specifications

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
$S0_{VDDQ}$	SD/ MMC/ CF I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
$S1_{VDDQ}$	SD/MMC I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
$S2_{VDDQ}$	GPIO/ CF I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO4}	GPIO/ I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply.
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C voltage supply	1.2	3.3	V	1.2-,1.8-, 2.5-, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	0.625 × VCC	VCC + 0.3	V	For $2.0\ V \le V_{CC} \le 3.6\ V$ (except USB port).VCC is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	VCC - 0.4	VCC + 0.3	V	For $1.7\ V \le V_{CC} \le 2.0\ V$ (except USB port). VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	0.25 × VCC	V	VCC is the corresponding I/O voltage supply.
V_{OH}	Output HIGH voltage	0.9 × VCC	–	V	I_{OH} (max) = –100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.
V_{OL}	Output LOW voltage	–	0.1 × VCC	V	I_{OL} (min) = +100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply.
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os that have a pull-up/down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD}
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at VDDQ
I_{CC} Core	Core and Analog Voltage Operating Current	–	200	mA	Total current through AVDD, VDD
I_{CC} USB	USB voltage supply operating current	–	60	mA	

Table 13. DC Specifications (continued)

Parameter	Description	Min	Max	Units	Notes
I_{SB1}	Total suspend current during Suspend Mode with USB 3.0 PHY enabled (L1 mode)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB2}	Total suspend current during Suspend Mode with USB 3.0 PHYdisabled (L2 mode)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB3}	Total Standby Current during Standby Mode (L3 mode)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB4}	Total Standby Current during Core Power Down Mode (L4 mode)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
V_{RAMP}	Voltage Ramp Rate on Core and I/O Supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise Level Permitted on VDD and I/O Supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise Level Permitted on AVDD Supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

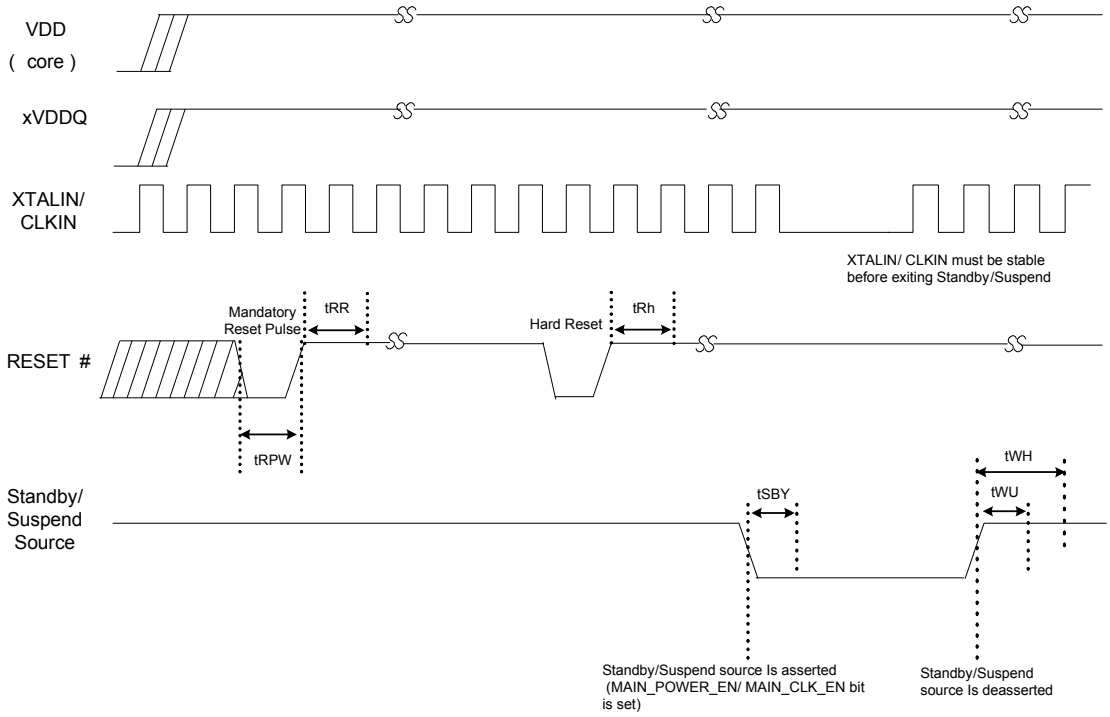
Reset Sequence

Table 14 provides the hard reset sequence requirements for SD3.

Table 14. Reset and Standby Timing Parameters

Parameter	Definition	Conditions	Min (ms)	Max (ms)
tRPW	Minimum RESET# pulse width	Clock Input	1	–
		Crystal Input	1	–
tRH	Minimum high on RESET#	–	5	–
tRR	Reset Recovery Time (after which Boot loader begins firmware download)	Clock Input	1	–
		Crystal Input	5	
tSBY	Time to enter Standby/Suspend (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set)	–	–	1
tWU	Time to wakeup from standby	Clock Input	1	–
		Crystal Input	5	–
tWH	Minimum time before Standby/Suspend source may be reasserted	–	5	–

Figure 7. Reset Sequence



Package Diagrams

Figure 8. 121-ball FBGA (10 × 10 × 1.20 mm) Package Outline, 001-54471

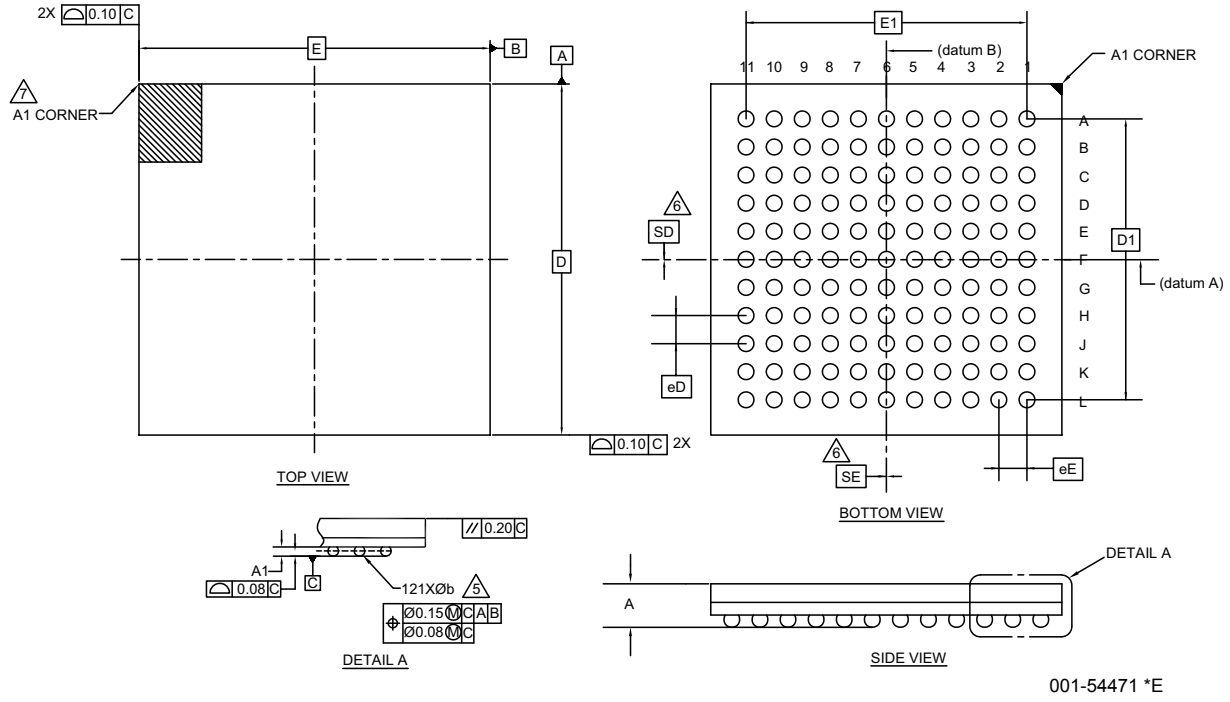
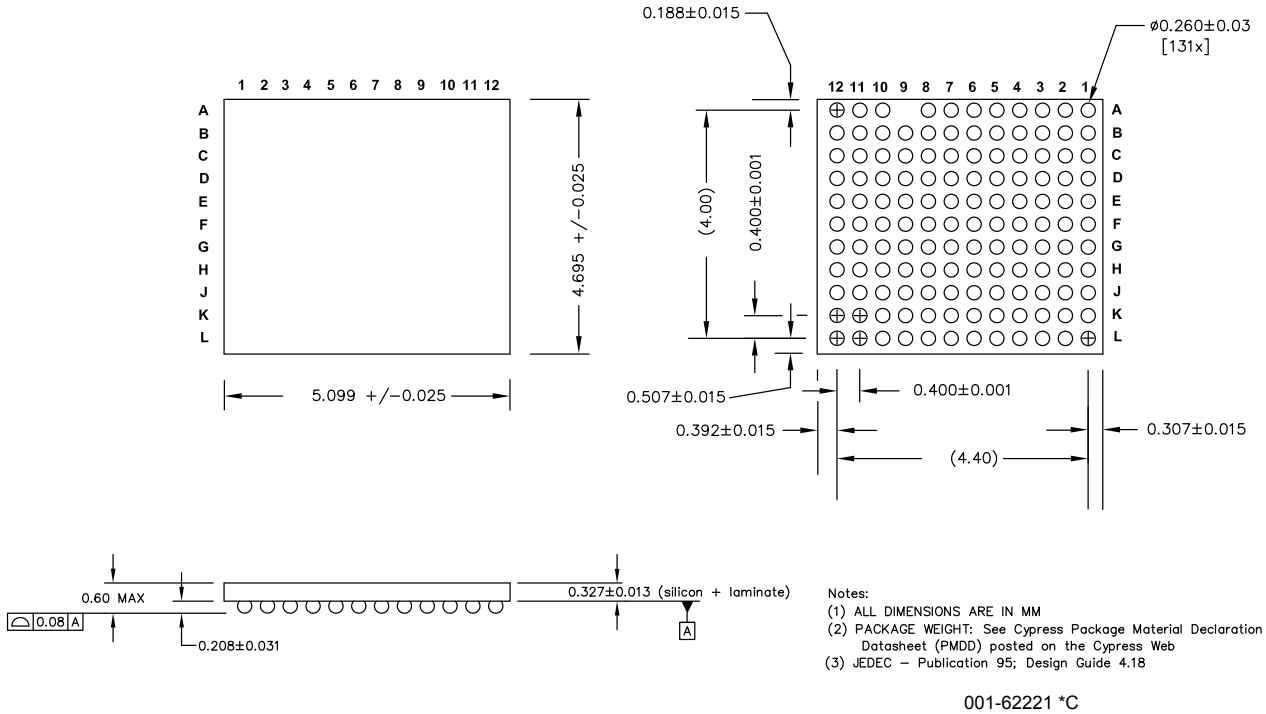


Figure 9. 131-ball WLCSP FB131/FN131 Package Outline, 001-62221

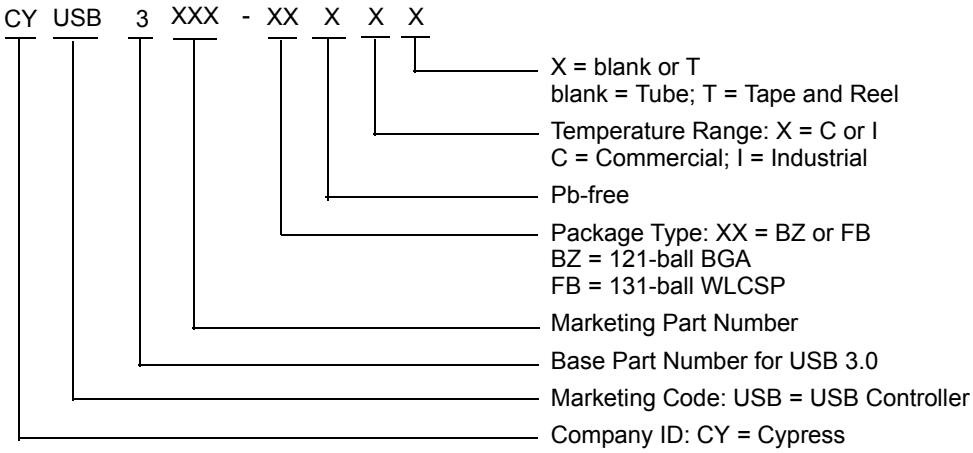


Ordering Information

Table 15. Ordering Information

Ordering Code	SD/eMMC SDIO Ports	SRAM (KB)	Package Type
CYUSB3023-FBXCT	1	512	131-ball WLCSP
CYUSB3025-BZXI	2	512	121-ball BGA

Ordering Code Definitions



Acronyms

Table 16. Acronyms Used in this Document

Acronym	Description
ACA	accessory charger adaptor
BGA	ball grid array
MMC	multimedia card
PLL	phase locked loop
SD	secure digital
SDIO	secure digital input / output
SLC	single-level cell
USB	universal serial bus

Document Conventions

Units of Measure

Table 17. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microamperes
µs	microseconds
mA	milliamperes
Mbps	Megabytes per second
MHz	mega hertz
ms	milliseconds
ns	nanoseconds
Ω	ohms
pF	pico Farad
V	volts

Errata

This document describes the errata for the SD3, CYUSB3021-BZXI. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CYUSB3021-BZXI	

SD3 USB and Mass Storage Peripheral Controller Qualification Status

Product Status: Sampling

SD3 USB and Mass Storage Peripheral Controller Errata Summary

The following table defines the errata applicability to available SD3 USB and Mass Storage Peripheral Controller family devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. USB Boot is Not Stable	CYUSB3021-BZXI	ES	Workaround provided Fix in Production Silicon

1. USB Boot is Not Stable

■Problem Definition

SD3 may not enumerate with the USB host (for example, a PC) and fail to boot from the USB port if, after reset, the PMODE pins are selected or configured to boot from USB.

■Parameters Affected

NA

■Trigger Condition(s)

This condition is triggered when PMODE pins are configured to boot from USB port.

■Scope of Impact

Fails to boot from USB Port

■Workaround

Select an alternate boot option, such as I2C or P-Port boot

■Fix Status

Fix in production silicon

Document History Page

Document Title: CYUSB302x, SD3™ USB and Mass Storage Peripheral Controller Document Number: 001-55190				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2761891	VSO	09/10/09	New data sheet.
*A	2823531	OSG	12/08/2009	Added data sheet to the USB 3.0 EROS spec 001-51884. No technical updates.
*B	3080927	OSG	11/08/2010	Changed status from Advance to Preliminary Added the following sections: Power, Configuration Fuse, Digital I/Os, EMI, System Level ESD, Absolute Maximum Ratings, AC Timing Parameters, Reset Sequence. Added DC Specifications table Updated Pin List Updated block diagram Updated part number Updated package diagram
*C	3204393	OSG	03/23/2011	Added a reference to footnote 1 in Table 1.
*D	3217917	OSG	04/06/2011	Changed values of R_USB2 and R_USB3
*E	3369042	OSG	12/06/2011	Updated tRR and tRPW for crystal input Added clarification regarding I_{OZ} and I_{IX} Updated 121-ball FBGA package diagram Added clarification regarding VCC in DC Specifications table In Power Modes description, stated that S2VDDQ cannot be turned off at any time if the S2-port is used in the application Updated Absolute Maximum Ratings Added requirement for by-pass capacitor on $U3RX_{VDDQ}$ and $U3TX_{VDDQ}$ Updated I2C interface tVD:ACK parameter for 1 MHz operation. Changed datasheet status from Preliminary to Final.
*F	3649782	OSG	08/16/2012	Added note about the I2C controller support for clock stretching. Updated Clocking and Hard Reset sections. Modified V_{BUS} min value. Updated Rise/fall time max value.
*G	3848148	OSG	12/20/2012	Updated 121-ball FBGA package diagram to current revision.
*H	4016006	GSZ	06/04/2013	Updated Features. Updated Applications. Updated Logic Block Diagram. Updated Functional Overview. Updated Pin Description for BGA. Added Pinout for WLCSP. Added Pin Description for WLCSP. Updated AC Timing Parameters Updated Package Diagrams (Added Figure 9). Updated Ordering Information (Updated part numbers).
*I	4131901	GSZ	09/23/2013	Changed status to Final. Updated Package Diagrams: spec 001-62221 – Changed revision from *B to *C. Updated Ordering Information (Updated part numbers). Updated in new template. Completing Sunset Review.
*J	5460202	RAJV	10/14/2016	Added Errata. Updated package diagram (spec 001-54471 *D to *E) in Package Diagrams. Updated CY Logo, Copyright and Disclaimer.

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